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OCT 2 3 2006

REMARKS/ARGUMENTS

In the Final action dated August 23, 2006, claims 1 – 23 were rejected. Applicant hereby requests reconsideration of the application in view of the below-provided remarks.

Claims 1 – 6, 8 – 11, 13 – 18, and 20 – 22 were rejected under 35 U.S.C. 103(a) as being unpatentable over Gilley (U.S. Pat. No. 6,215,876), in view of Pozidis (U.S. PG-Pub. No. 20030005383), and further in view of Johnson et al. (U.S. Pat. No. 6,587,804, hereinafter Johnson). Claims 7, 12, 19, and 23 were rejected under 35 U.S.C. 103(a) as being unpatentable over Gilley, in view of Pozidis, and further in view of Johnson, and further in view of Yoshimura (U.S. Pat. No. 5,123,020).

Claim 1

Claim 1 recites:

> "A bit error detection circuit comprising:
> a predictor circuit that uses a plurality of bits of a bit sequence to predict a next bit in the sequence;
> a comparator circuit that compares an actual next bit in the sequence with the predicted next bit to determine whether there is any error in the actual next bit; and
> ***a correction circuit that corrects any error in the actual next bit to provide a corrected actual next bit.***" (emphasis added)

With regard to claim 1, the Office action states that Gilley teaches predictor logic and a comparator circuit, but that Gilley fails to teach a correction circuit. Pozidis is cited for teaching a correction circuit. Applicant asserts that claim 1 is not rendered obvious from Gilley in view of Pozidis and Johnson because 1) the Office action has not provided a teaching, suggestion, or motivation to combine Pozidis with Gilley and 2) Gilley teaches away from combining Pozidis with Gilley.

Gilley does not provide a teaching, suggestion, or motivation to use a ***correction circuit*** as recited in claim 1

The correction circuit recited in claim 1 is deemed to be taught by Pozidis. As stated in *Ex parte Clapp*, 227 USPQ 972, (Bd. Pat. App. & Inter. 1985) "[t]o support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." Additionally, "[t]he examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness." [M.P.E.P. 2142]

Gilley does not expressly or impliedly suggest the claimed invention - The Final action cites Gilley, col. 7, lines 1 – 5 as providing a suggestion to use a correction circuit as taught by Pozidis and as recited in claim 1. At col. 7, lines 1 – 5, Gilley recites:

> "if the number of errors is large (e.g. ≥ 4 bit errors) (66/76), it is concluded that the predicted IV is wrong (76), and appropriate action can be taken (78), which might consist of dropping crypto-sync and attempting to re-acquire it from the received IV (80)."

Although Gilley discloses that "an appropriate action can be taken," nowhere does Gilley expressly or impliedly suggest "a correction circuit that corrects any error in the actual next bit to provide a corrected actual next bit" as recited in claim 1. Applicant points out that the test for obviousness in not whether the prior art suggests some alternative action, but whether or not the prior art suggests the claimed invention. The phrase "appropriate action can be taken" is not an express or implied suggestion of the claimed invention, i.e., a correction circuit.

Gilley does teach that an appropriate action may consist of "dropping crypto-sync and attempting to acquire it from the received IV." While Gilley does teach one action that can be taken, nowhere does Gilley expressly or impliedly suggest the claimed invention.

The Final action does not provide a convincing line of reasoning as to why the artisan would have found the claimed invention obvious in light of the teachings of the references - The Final action cites, as support for the combination of Gilley and Pozidis, the conclusory statement:

> "[i]t would have been obvious to one of ordinary skill in the art at the time the invention was made to use a corrector circuit to correct the bits in Gilley's invention, since one of ordinary skill in the art would have realized that enabling Gilley's invention to correct bits would have made the invention more beneficial and would have allowed Gilley to generate vectors with greater accuracy." (Final action, page 4) (emphasis added)

This conclusory statement is unsupported by any facts. Further, Applicant asserts that the statement does not present a convincing line of reasoning as to why an artisan would have found the claimed invention obvious. The support provided for the Examiner's suggested combination includes the specific statement, "since one of ordinary skill in the art would have realized that enabling Gilley's invention to correct bits would have made the invention more beneficial and would have allowed Gilley to generate vectors with greater accuracy." This statement basically says that an artisan would have selected a correction circuit to make the invention better. Applicant asserts that making an invention better does not provide a convincing line of reasoning to support a *prima facie* case of obviousness.

Gilley Teaches Away from using a Correction Circuit

Applicant asserts that Gilley teaches away from using a correction circuit and therefore teaches away from the combination of Gilley and Pozidis. As evidence that Gilley teaches away from a correction circuit, Gilley discloses at column 5, lines 21 – 30 that the preferred embodiment achieves a stated objective of maintaining crypto-sync (column 6, line 49) "without error correction." That is, the technique disclosed by Gilley expressly avoids error correction. Applicant asserts that a technique that expressly avoids error correction teaches away from combining Gilley with a reference, such as Pozidis, for its error correction teaching.

Further, in contrast to Applicant's claim 1, Gilley teaches *ignoring* or coasting by the received IV *in the presence of bit errors*. For example, Gilley states:

> "Coasting systems ... (a) predict the correct IV, (b) detect if the received IV does not match the predicted IV and, further, (c) if so, ignore or coast by the received IV .... The preferred embodiment therefore utilizes ... coasting ... in the presence of bit errors to transmitted IV caused by the communications channel ... ." (col. 5, lines 20-28)

That is, Gilley teaches ignoring bit errors when the number of bit errors is small instead of using *a correction circuit* that *corrects any error* in the actual next bit to provide a *corrected* actual next bit, thereby teaching away from the claimed invention. Teaching away from the claimed invention by a reference is a *per se* demonstration of lack of *prima facie* obviousness.

Dependent claim 2

Claim 2 recites that the correction circuit "comprises a circuit element that ***replaces the actual next bit with the corrected actual next bit*** in the plurality of bits." The limitations of claim 2 are rejected as being taught by Pozidis. The logic for combining Pozidis with Gilley is the same as the logic provided with respect to claim 1. Because of the similarities between the rejections of claims 1 and 2, Applicant asserts that the remarks provided above with respect to claim 1 apply also to claim 2.

Dependent claim 3

Dependent claim 3 is dependent on claim 1. Applicant asserts that claim 1 is allowable at least based on an allowable claim 1.

Dependent claim 4

Claim 4 recites that the bit error detection circuit of claim 1 further includes "***a trigger circuit that activates the correction circuit when the predictor circuit contains a plurality of bits in which no erroneous bits have been detected.***" The support for the rejection of claim 4 is "(Figure 4 #68, columns 6, lines 46 – 57, it should be noted that the Figure 4 #64, will trigger the correction circuit which will be placed at Figure 4 #78)." (Final action, page 6) Applicant asserts that Gilley does not

teach or suggest a correction circuit and Gilley explicitly states that the preferred embodiment achieves the stated objective of maintaining crypto-sync "without error correction." Because Gilley does not teach or suggest error correction, it follows that a trigger circuit that activates a correction circuit is not taught or suggested by Gilley.

In the Final action, Fig. 4, #68 and column 6, lines 46 – 57 of Gilley are cited as teaching the limitations of claim 4. Elements 64, 66, and 68 of Fig. 4 teach that when no bit errors are detected, it should be assumed that the received and predicted initialization vectors are correct. These elements, particularly element 68, teach nothing about a trigger circuit that "activates the correction circuit when the predictor circuit contains a plurality of bits in which no erroneous bits have been detected" as recited in claim 4.

Dependent claims 5, 6, and 7

Dependent claims 5, 6, and 7 include limitations related to the trigger circuit recited in claim 4. Because, as described above, Gilley does not disclose a correction circuit or a trigger circuit that activates the correction circuit, Applicant asserts that Gilley does not teach or suggest the limitations related to the trigger circuit.

Claim 8

Claim 8 recites:

> "A bit error detection circuit comprising:
> a shift register that receives N bits of a pseudo-random bit sequence (PRBS);
> a first logic element that receives output signals from two stages of the shift register and provides a signal indicative of a predicted (N+1)-th bit;
> a second logic element that receives the signal indicative of the predicted (N+1)-th bit and a signal indicative of an actual (N+1)-th bit and provides an output signal indicative of any error in the actual (N+1)-th bit; and
> a third logic element that receives the output signal and corrects the actual (N+1)-th bit according to the output signal as the (N+1)-th bit propagates through the shift register. " (emphasis added)

Claim 8 is rejected under the same logic as claim 1. Because of the similarities between claims 1 and 8, Applicant asserts that the remarks provided above with reference to claim 1 apply also to claim 8.

Dependent claims 9 – 13

Dependent claim 9 has similar limitations to dependent claim 2 and therefore the remarks provided above with reference to claim 2 apply also to claim 9.

Dependent claim 10 has similar limitations to dependent claim 4 and therefore the remarks provided above with reference to claim 4 apply also to claim 10.

Dependent claims 11 and 12 include limitations related to the trigger circuit recited in claim 10. Because, as described above, Gilley does not disclose correction logic or a trigger circuit that activates the correction logic, Applicant asserts that Gilley does not disclose the limitations related to the trigger circuit.

Dependent claim 13 has similar limitations to dependent claim 4 and therefore the remarks provided above with reference to claim 4 apply also to claim 13.

Claims 14, 21, and 22

Claims 14, 21, and 22 include limitations that are similar to the limitations in claim 1. These claims are rejected under the same logic as claim 1. Because of the similarities between claims 1 and claims 14, 21, and 22, Applicant asserts that the remarks provided above with reference to claim 1 apply also to these claims.

Dependent claims 15 – 20

Dependent claim 15 has similar limitations to dependent claim 2 and therefore the remarks provided above with reference to claim 2 apply also to claim 15.

Dependent claim 17 has similar limitations to dependent claim 4 and therefore the remarks provided above with reference to claim 4 apply also to claim 17.

Dependent claims 16 and 18 – 20 are dependent on claim 14. Applicant asserts that these claims are allowable at least based on an allowable claim 14.

Independent claim 23

Independent claim 23 includes limitations similar to claim 1. Because of the similarities between claims 1 and 23, Applicant asserts that the remarks provided above with reference to claim 1 apply also to claim 23.

Applicant respectfully requests reconsideration of the claims in view of the remarks made herein. A notice of allowance is earnestly solicited.

Respectfully submitted,

Date: October 23, 2006

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